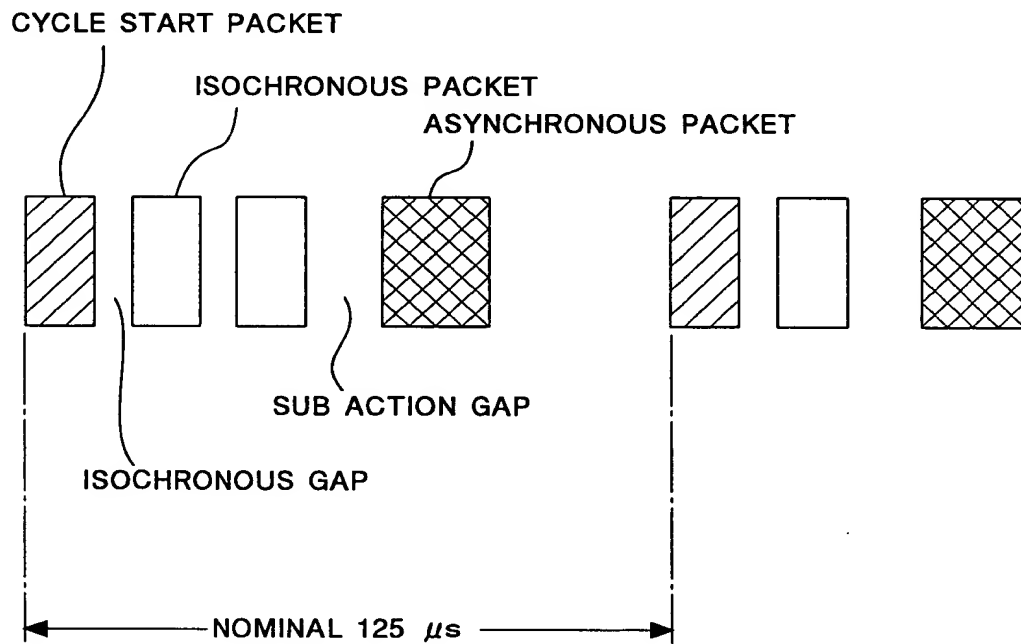
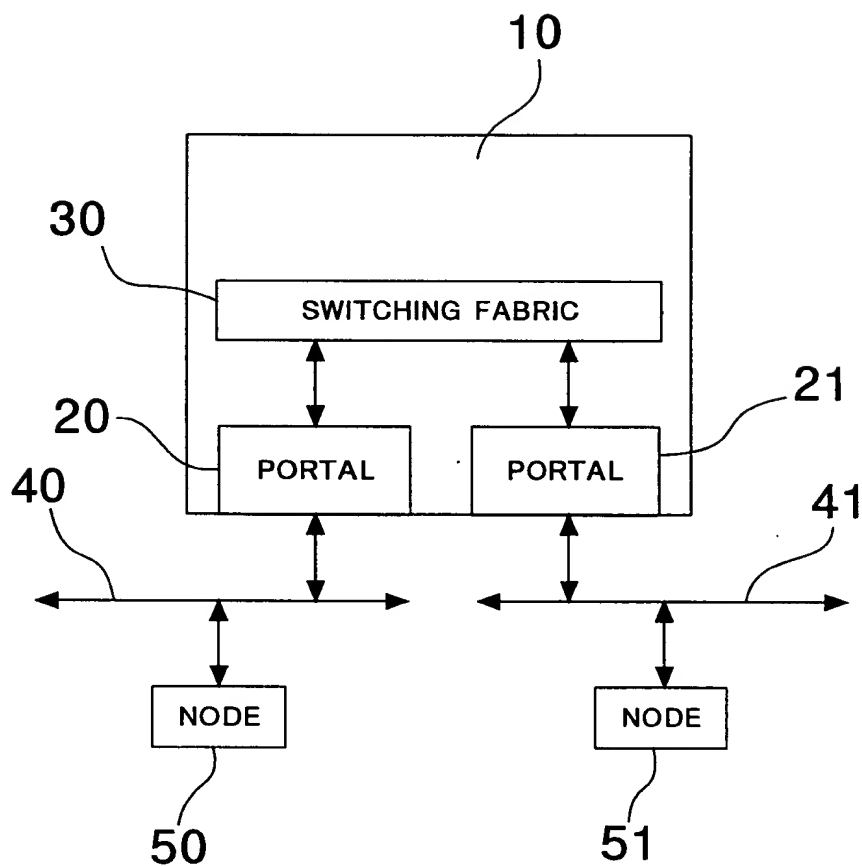


FIG. 1



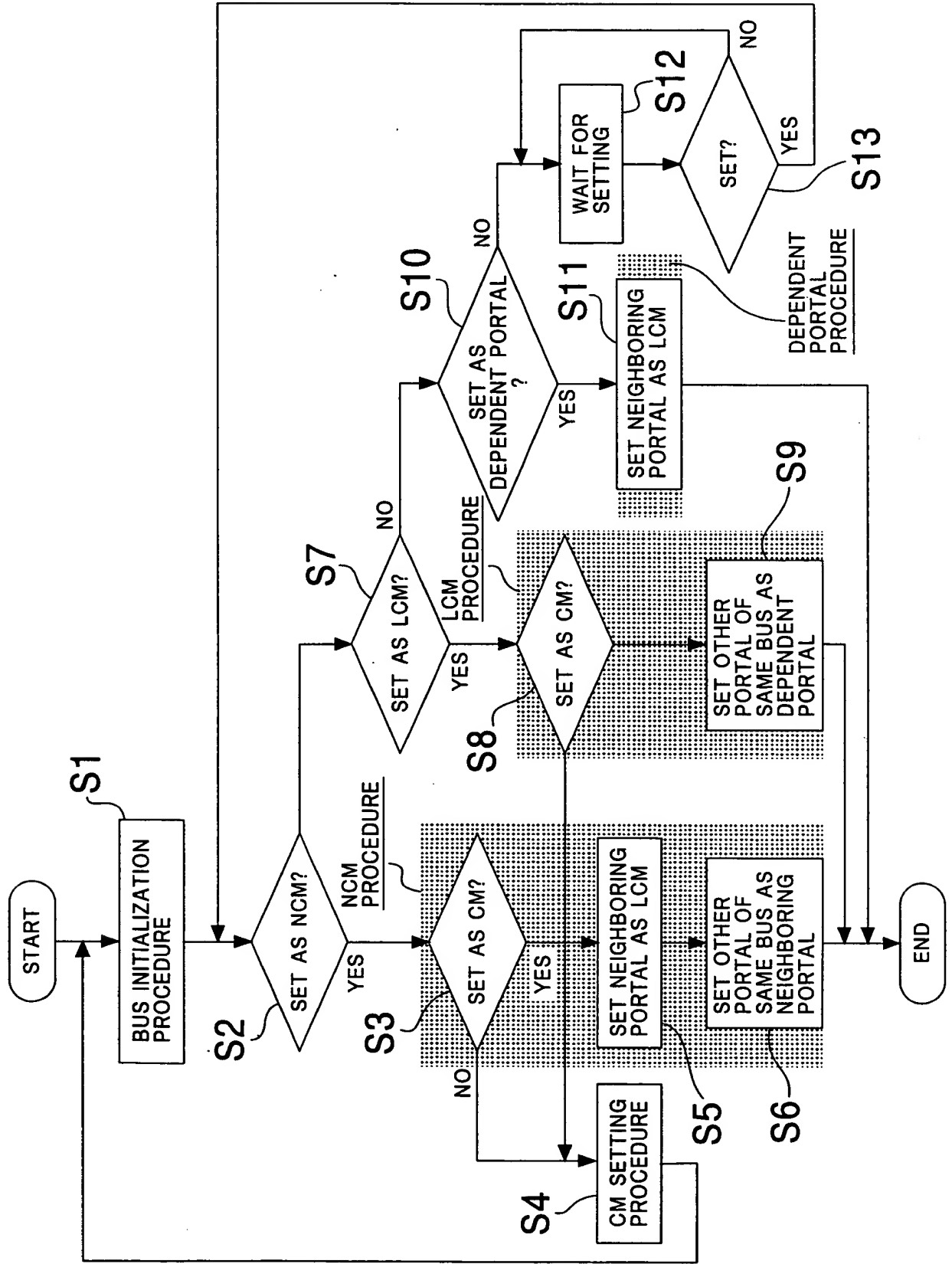
00240-001560

FIG.3



The diagram illustrates a network architecture where a central **NETWORK CYCLE MASTER 10** is connected to three **LOCAL CYCLE MASTERS** (40, 42, and 44) via a common bus 41. The network master 10 consists of two nodes, A and B. Node A is connected to the bus 41, and node B is connected to a **SYNCHRONIZING SIGNAL** block. This block sends synchronizing signals to the bus 41, which then distributes them to the three local cycle masters. Each local cycle master (40, 42, and 44) also consists of two nodes (C/D, E/F, and G/H respectively) and a **SYNCHRONIZING SIGNAL** block. The bus 41 is labeled with numbers 40, 41, 42, 43, and 44 at various points along its length.

FIG. 5



[illegible]

FIG.7

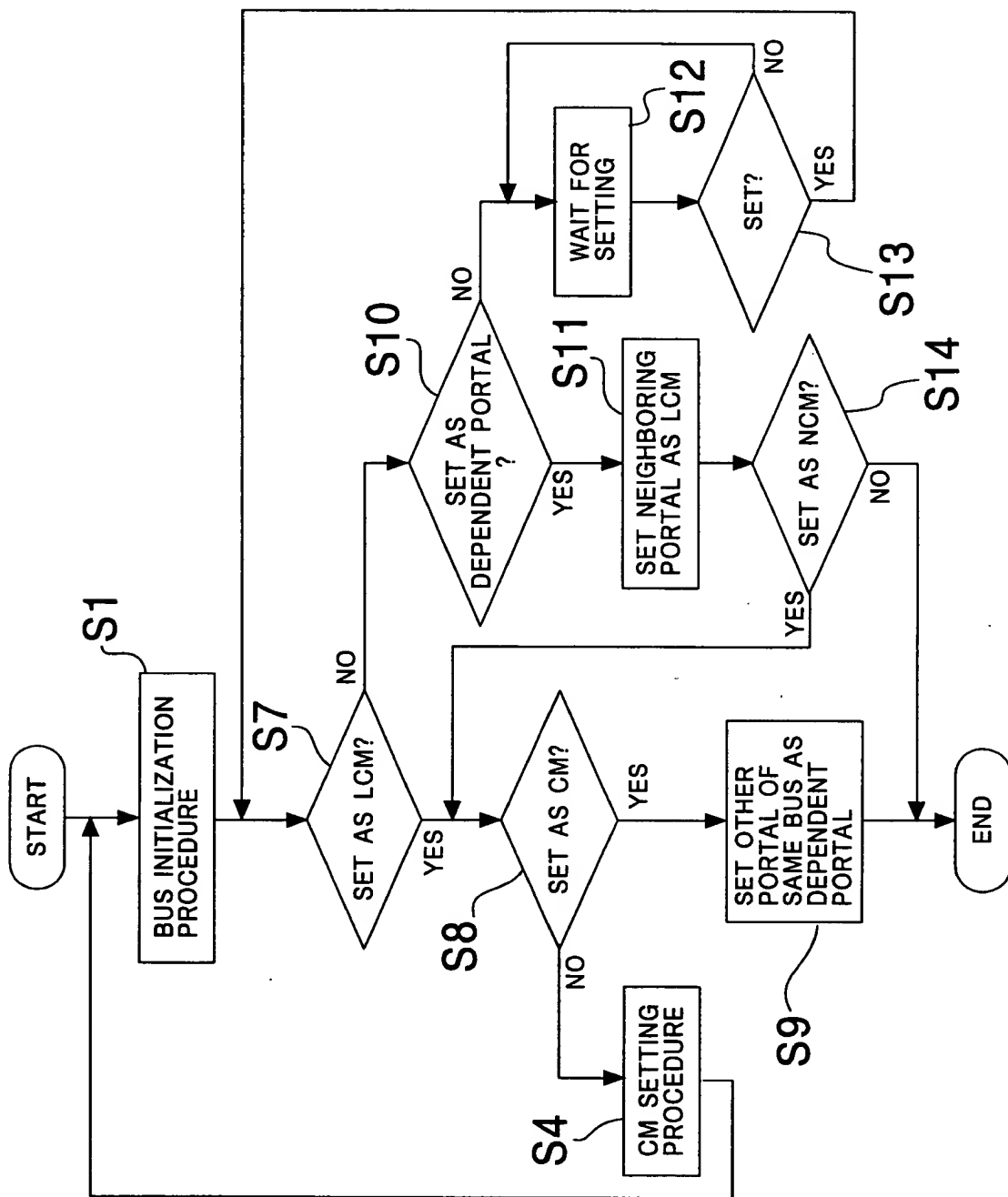


FIG. 8

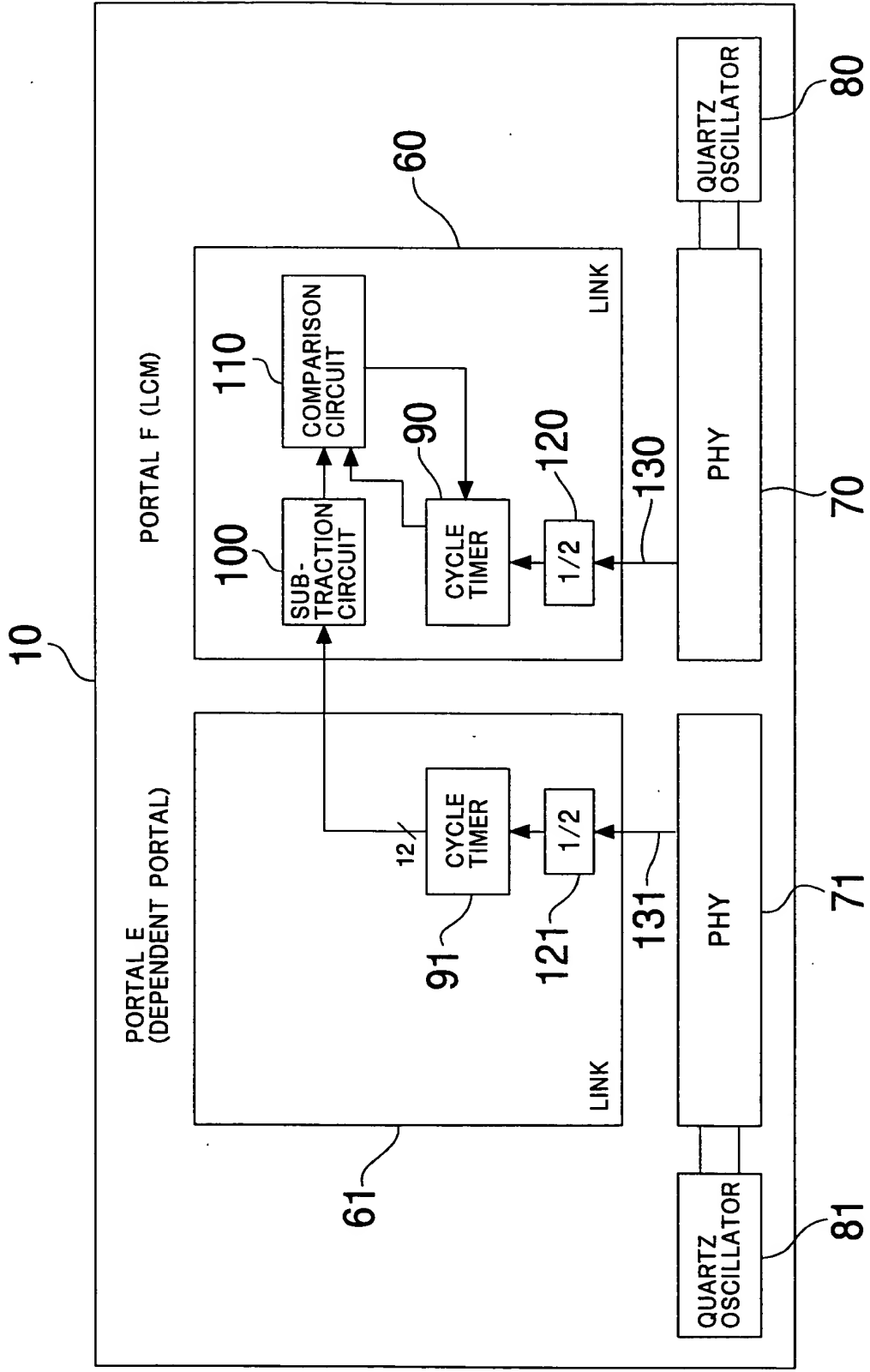
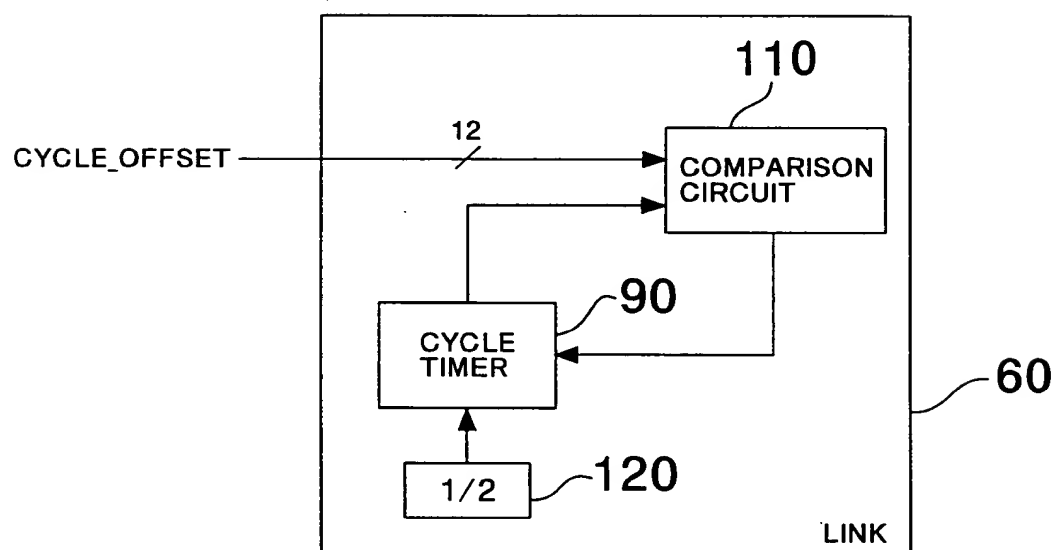


FIG.9

INPUT FROM SUBTRACTION CIRCUIT 100	OUTPUT OF COMPARISON CIRCUIT 110
GREATER THAN 0	01_2 (fast)
0	00_2 (stay)
SMALLER THAN 0	10_2 (slow)

002440-004550

FIG.10



002400049900

FIG. 11

INPUTTED CYCLE_OFFSET	OUTPUT OF COMPARISON CIRCUIT 110
GREATER THAN 0 BUT SMALLER THAN 1,536	01 ₂ (fast)
0	00 ₂ (stay)
EQUAL TO OR GREATER THAN 1,536	10 ₂ (slow)

FIG.12

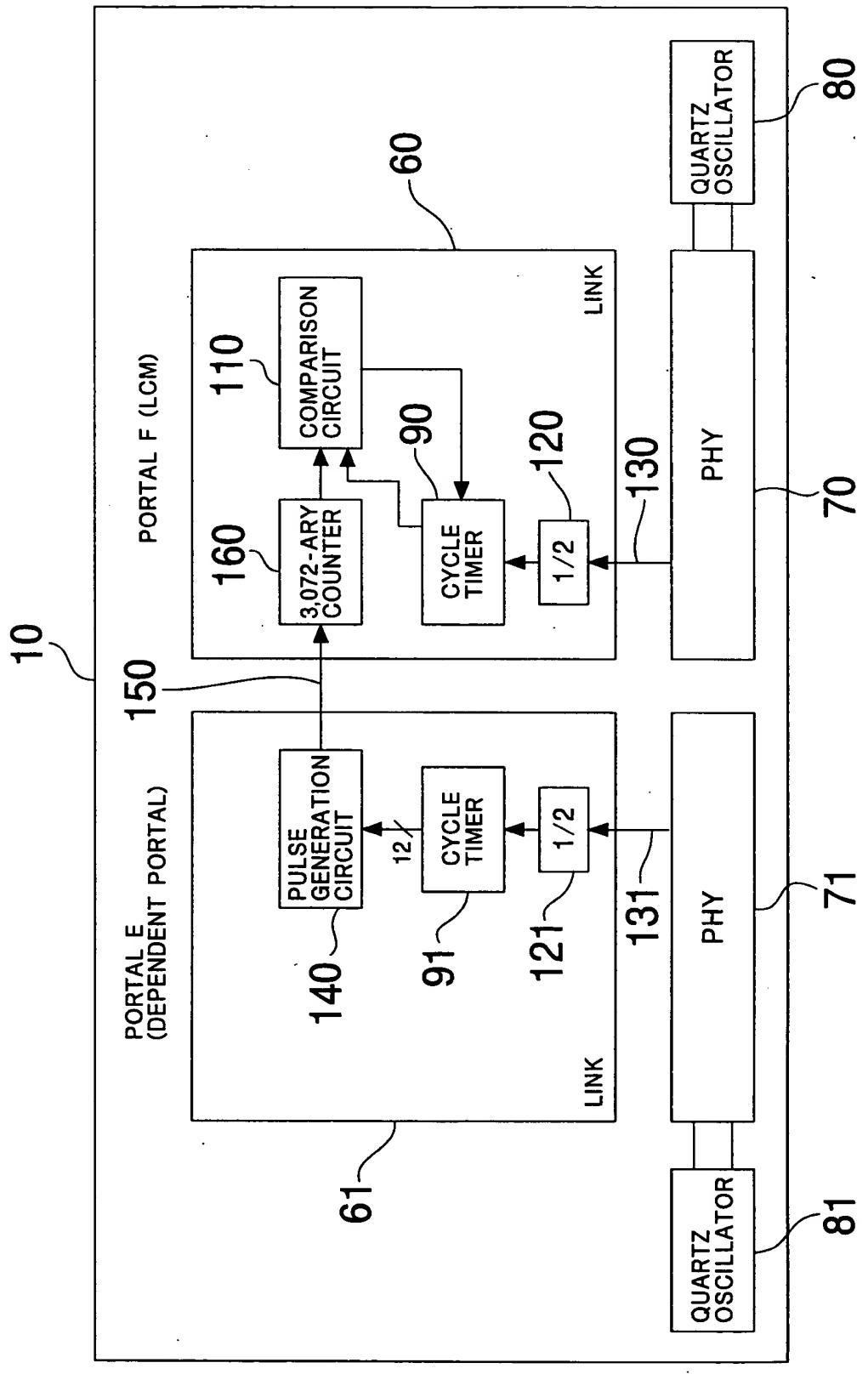


FIG. 13

